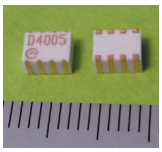
CDKD LTCC Multi-layered Differential Delay Lines

CDKD-type delay line is an LTCC (Low Temperature Co-fired Ceramic) chip-type differential delay line, also due to ELMEC's own high-density monolithic LC structure.

FEATURES

- Crosstalk is reduced and, even for GHz-level high-speed signals, it can maintain stable, differential impedance and by connecting the 2 differential lines, can also be used as a 2x Td single-ended Delay Line.
- It is a RoHS-compliant component.



COMMON SPECIFICATIONS

Impedance:	single-ended: 50Ω±10% / differential: 100Ω±10%
Waveform Distortion:	Overshoot/preshoot under 20%
Delay Time Temp. Coefficient:	0~150ppm/°C
Insulation Resistance:	DC50V, over 100MΩ
Operating Temperature Range:	-40°C to +85°C
Storage Temperature Range:	-40°C to +120°C

SPECIFICATIONS

Part Number	Delay Time	Delay Difference	Rise/Fall Time (20%-80%)	-3dB Passband		DC Resistance
				Actual(1)*	Guarantee(2)*	
CDKD0105	100ps±50ps	10ps Max.	100ps Max.	DC～10GHz	DC～3GHz	1.0Ω Max.
CDKD0205	200ps±50ps	10ps Max.	100ps Max.	DC～10GHz	DC～3GHz	
CDKD0305	300ps±50ps	10ps Max.	100ps Max.	DC～10GHz	DC～3GHz	
CDKD0405	400ps±50ps	10ps Max.	100ps Max.	DC～7.5GHz	DC～3GHz	1.5Ω Max
CDKD0505	500ps±50ps	10ps Max.	100ps Max.	DC～6GHz	DC～3GHz	
CDKD0605	600ps±50ps	10ps Max.	100ps Max.	DC～5GHz	DC～3GHz	3.0Ω Max.
CDKD0705	700ps±50ps	10ps Max.	110ps Max.	DC～4.3GHz	DC～3GHz	
CDKD0805	800ps±50ps	10ps Max.	120ps Max.	DC～3.8GHz	DC～3GHz	
CDKD0905	900ps±50ps	10ps Max.	130ps Max.	DC～3.3GHz	DC～2.7GHz	3.5Ω Max.
CDKD1005	1.0ns±50ps	10ps Max.	150ps Max.	DC～3GHz	DC～2.4GHz	
CDKD1105	1.1ns±55ps	15ps Max.	160ps Max.	DC～2.7GHz	DC～2.2GHz	4.0Ω Max.
CDKD1205	1.2ns±60ps	15ps Max.	180ps Max.	DC～2.5GHz	DC～2GHz	
CDKD1305	1.3ns±65ps	15ps Max.	190ps Max.	DC～2.3GHz	DC～1.9GHz	4.5Ω Max.
CDKD1405	1.4ns±70ps	15ps Max.	210ps Max.	DC～2.1GHz	DC～1.7GHz	
CDKD1505	1.5ns±75ps	15ps Max.	220ps Max.	DC～2GHz	DC～1.6GHz	4.0Ω Max.
CDKD1605	1.6ns±80ps	20ps Max.	240ps Max.	DC～1.9GHz	DC～1.5GHz	
CDKD1805	1.8ns±90ps	20ps Max.	270ps Max.	DC～1.7GHz	DC～1.3GHz	4.5Ω Max.
CDKD2005	2.0ns±100ps	20ps Max.	300ps Max.	DC～1.5GHz	DC～1.2GHz	5.0Ω Max.
CDKD2505	2.5ns±125ps	25ps Max.	360ps Max.	DC～1.2GHz	DC～960MHz	
CDKD3005	3.0ns±150ps	30ps Max.	400ps Max.	DC～1.1GHz	DC～880MHz	
CDKD3505	3.5ns±175ps	40ps Max.	510ps Max.	DC～860MHz	DC～690MHz	6.0Ω Max.
CDKD4005	4.0ns±200ps	50ps Max.	600ps Max.	DC～750MHz	DC～600MHz	7.5Ω Max.
CDKD4505	4.5ns±225ps	50ps Max.	660ps Max.	DC～660MHz	DC～530MHz	
CDKD5005	5.0ns±250ps	50ps Max.	720ps Max.	DC～600MHz	DC～480MHz	

(1)* In order to achieve the Actual -3dB passband, it is necessary to input a differential signal into the suggested land pattern.
(2)* The guaranteed value of -3dB passband is limited by the band width of the pin probe during product inspection.

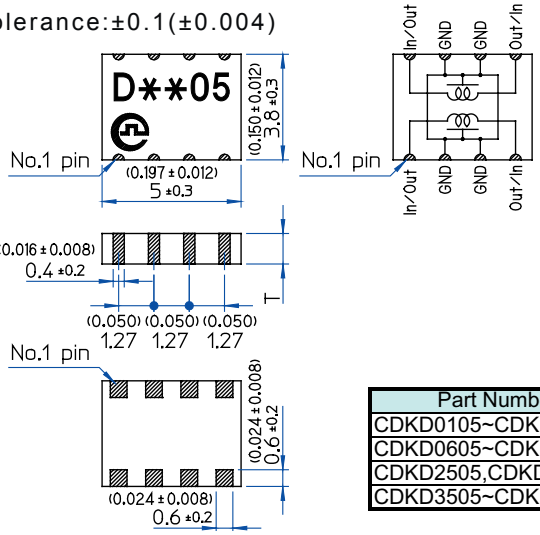
＊By connecting the 2 differential lines, can also be used as a single-ended delay line. Please see the CDM page for more information.

CDKD LTCC Multi-layered Differential Delay Lines

PACKAGE DIMENSIONS & PIN CONFIGURATION

Unit:mm (inch)

Tolerance:±0.1(±0.004)

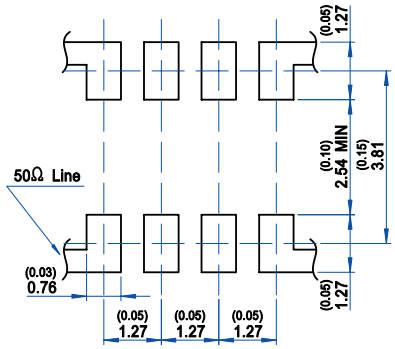


Part Number	Dimension of T
CDKD0105~CDKD0505	1.0Max (0.039Max)
CDKD0605~CDKD2005	2.0Max (0.079Max)
CDKD2505,CDKD3005	2.5Max (0.098Max)
CDKD3505~CDKD5005	3.0Max (0.118Max)

SUGGESTED LAND PATTERN

Unit:mm (inch)

Tolerance:±0.1(±0.004)

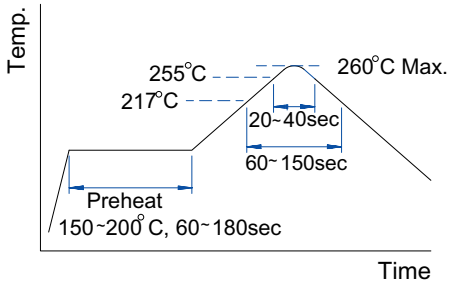


REFLOW SOLDERING CONDITIONS

Storage conditions are as per MSL1. These component families are not moisture-sensitive.

Baking prior to reflow is not required.

J-STD-020C Pb-Free Standard

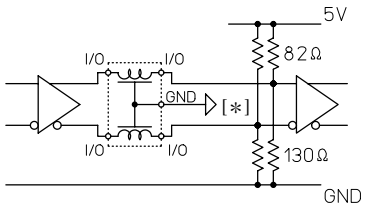


Note: Published specifications are subject to change without prior notice.

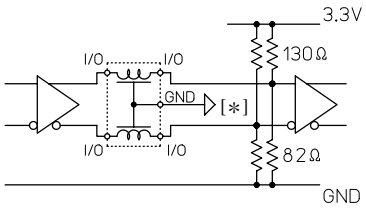
CDKD LTCC Multi-layered Differential Delay Lines

TYPICAL APPLICATIONS AND TERMINATION METHODS

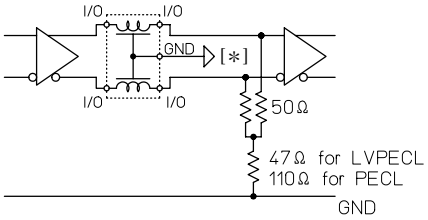
(1) PECL



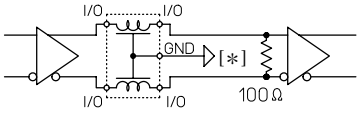
(2) LVPECL



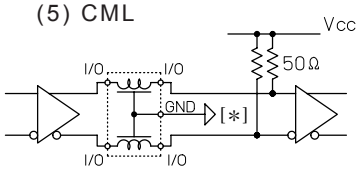
(3) Twisted Pair Termination



(4) LVDS



(5) CML

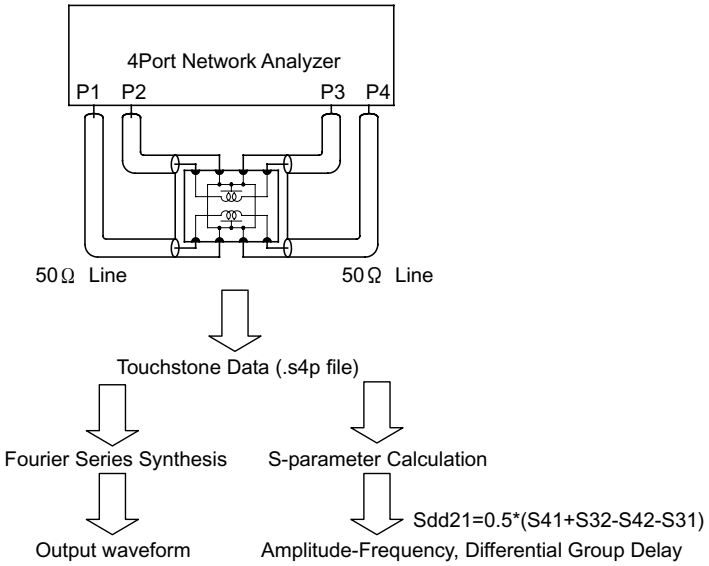


[*] Signal GND potential, such as a power supply GND or a Vcc line.

Note: The Delay Line can be used with the GND disconnected, however, in order to obtain superior performance, we recommend that all GND pins should be connected.

OUTPUT WAVEFORMS (1)

Measurements Circuit and Data Plot Procedure

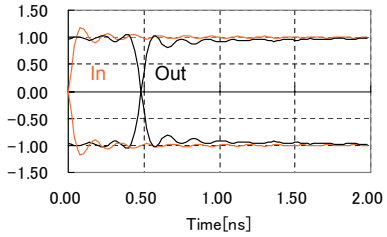


CDKD LTCC Multi-layered Differential Delay Lines

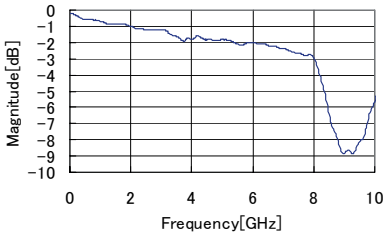
OUTPUT WAVEFORMS (2)

(1) CDKD0505

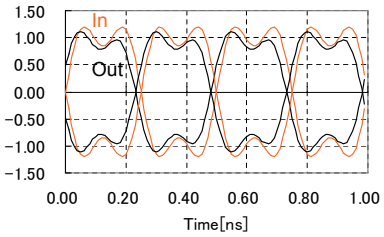
Output waveform (Step function)



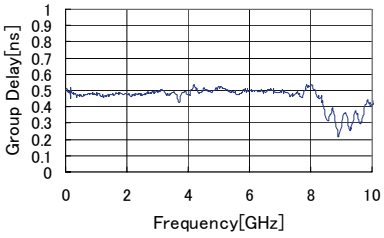
Sdd21 Amplitude / Frequency



Output waveform (2GHz Clock)

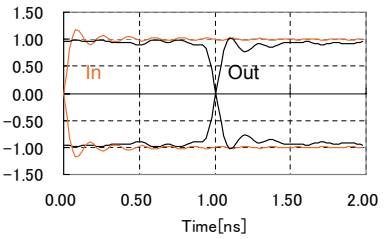


Group Delay

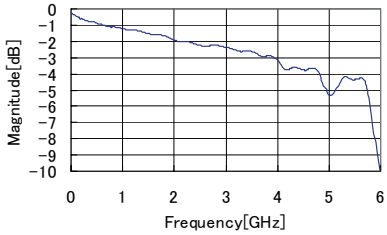


(2) CDKD1005

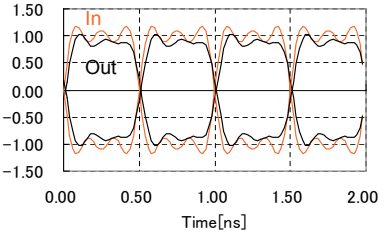
Output waveform (Step function)



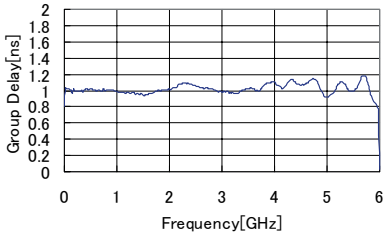
Sdd21 Amplitude / Frequency



Output waveform (1GHz Clock)



Group Delay

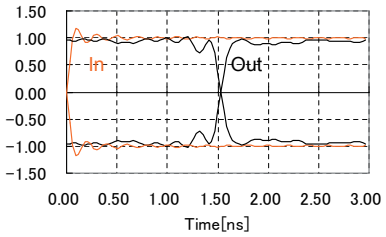


CDKD LTCC Multi-layered Differential Delay Lines

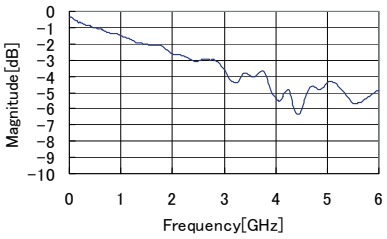
OUTPUT WAVEFORMS (3)

(3) CDKD1505

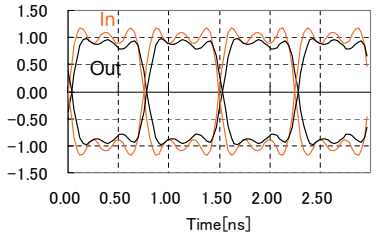
Output waveform (Step function)



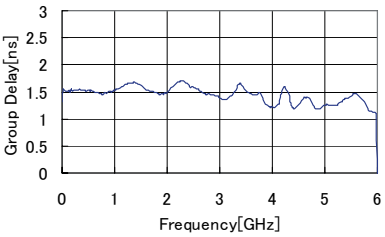
Sdd21 Amplitude / Frequency



Output waveform (667MHz Clock)

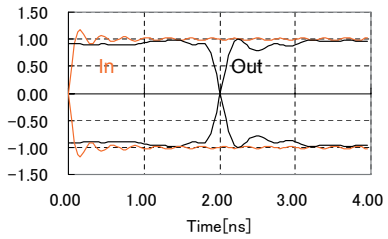


Group Delay

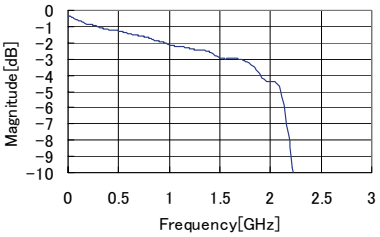


(4) CDKD2005

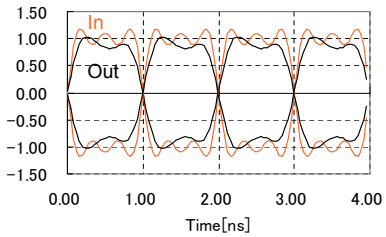
Output waveform (Step function)



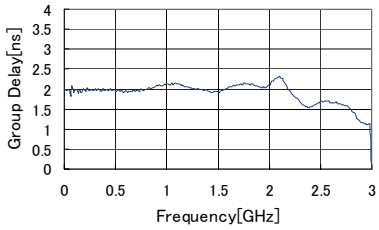
Sdd21 Amplitude / Frequency



Output waveform (500MHz Clock)



Group Delay

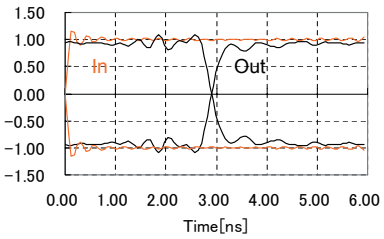


CDKD LTCC Multi-layered Differential Delay Lines

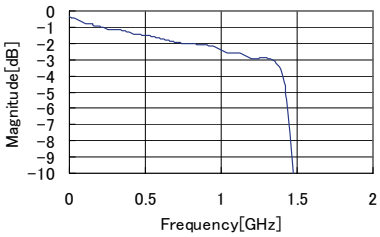
OUTPUT WAVEFORMS (4)

(5) CDKD3005

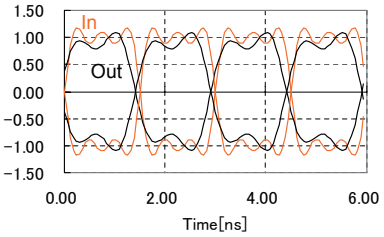
Output waveform (Step function)



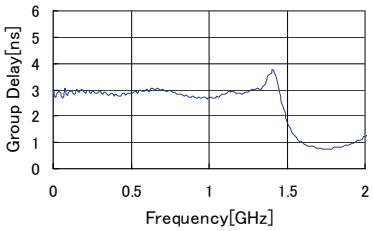
Sdd21 Amplitude / Frequency



Output waveform (333MHz Clock)

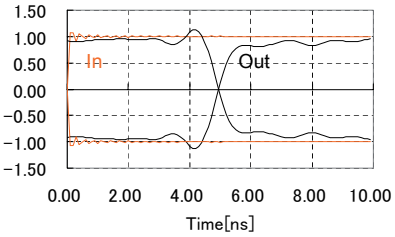


Group Delay

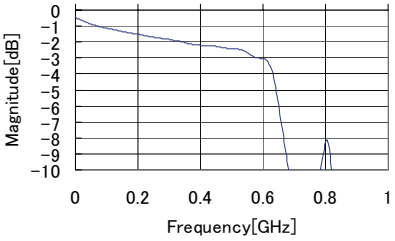


(6) CDKD5005

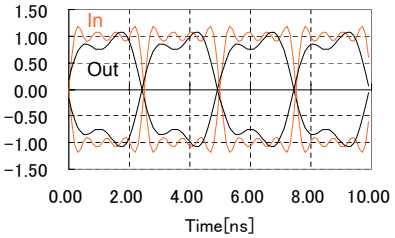
Output waveform (Step function)



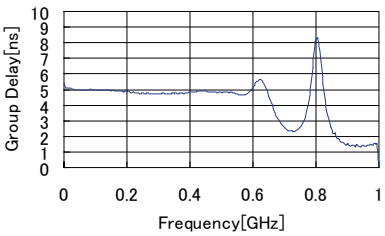
Sdd21 Amplitude / Frequency



Output waveform (200MHz Clock)



Group Delay



RoHS Compliance Status

Initially developed only as a RoHS-compliant component.