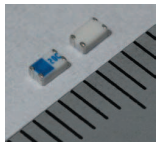
Differential Delay Lines

CDLF 0805 Size Differential Chip Delay Line

FEATURES

- Smaller & lower cost than our existing products
- 10ps increments
- 15GHz Band width, available for 10Gbps data signals
- Suitable for inter-lane de-skew on multi-lane high speed serial transmission
- Solves the problems of space usage and the characteristic degradation of the substrate trace.
  (Please See Technical Note)
- Based on your requirements, 2012 size single-ended Delay Lines are also possible.



SPECIFICATIONS

Input/Output Impedance:	Differential 100Ω±10% *
Waveform Distortion:	Overshoot/preshoot under ±20%
Insulation Resistance:	DC50V, over 100MΩ
Durable Voltage:	DC50V, 1 minute
Rated Current:	50mA
Rated Voltage:	5V
Operating Temperature Range:	-40°C to +85°C
Storage Temperature Range:	-40°C to +120°C

* Single-ended operation will not produce usable waveforms.

Part Number	Delay Time	Rise/Fall Time(1)*		-3dB Passband		DC
		Actual(2)*	Guarantee(3)*	Actual(2)*	Guarantee(3)*	Resistance
CDLF01C	10ps±5ps	20ps Typ.	40ps Max.	DC～20GHz	DC～15GHz	0.5Ω Max.
CDLF02C	20ps±5ps	20ps Typ.	40ps Max.	DC～20GHz	DC～15GHz	0.5Ω Max.
CDLF03C	30ps±5ps	20ps Typ.	40ps Max.	DC～20GHz	DC～15GHz	1.0Ω Max.
CDLF04C	40ps±5ps	20ps Typ.	40ps Max.	DC～20GHz	DC～15GHz	1.0Ω Max.
CDLF05C	50ps±5ps	20ps Typ.	40ps Max.	DC～20GHz	DC～15GHz	1.0Ω Max.
CDLF10C	100ps±10ps	20ps Typ.	40ps Max.	DC～20GHz	DC～15GHz	1.5Ω Max.
CDLF15C	150ps±10ps	25ps Typ.	50ps Max.	DC～18GHz	DC～12GHz	1.8Ω Max.
CDLF20C	200ps +10ps/−20ps	25ps Typ.	50ps Max.	DC～15GHz	DC～11GHz	2.5Ω Max.
CDLF30C	300ps +10ps/−20ps	30ps Typ.	60ps Max.	DC～10GHz	DC～7GHz	3.5Ω Max.

(1)* 20%-80%
(2)* Using the recommended Land Pattern, when there is no skew in the differential input signal.
(3)* Restricted value due to the test fixture.

Recommended combination for 60ps～90ps, 110ps～140ps and 160ps～190ps interpolation

Delay Time	Combination	Delay Time	Combination	Delay Time	Combination
60ps	CDLF03C ×2	110ps	CDLF01C+CDLF10C	160ps	CDLF01C+CDLF15C
70ps	CDLF03C+CDLF04C	120ps	CDLF02C+CDLF10C	170ps	CDLF02C+CDLF15C
80ps	CDLF04C ×2	130ps	CDLF03C+CDLF10C	180ps	CDLF03C+CDLF15C
90ps	CDLF04C+CDLF05C	140ps	CDLF04C+CDLF10C	190ps	CDLF04C+CDLF15C

We can provide the products for delay times shown in the table above, subject to volume requirements.

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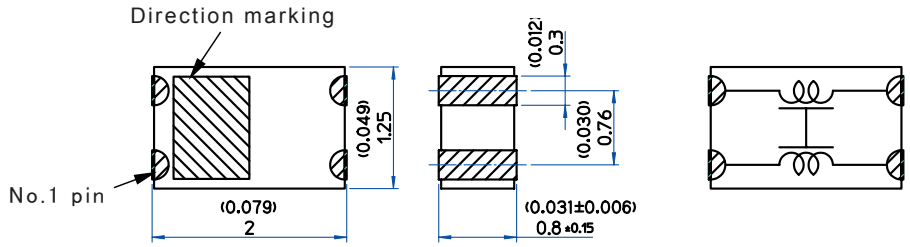
PACKAGE DIMENSIONS & PIN CONFIGURATION

Unit:mm (inch)

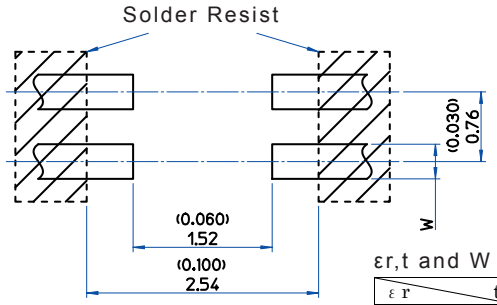
Tolerance:±0.1(±0.004)



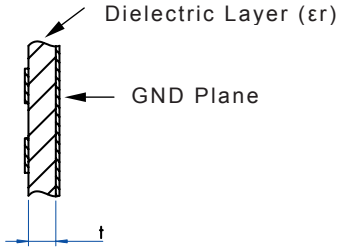
SUGGESTED LAND PATTERN

Unit:mm (inch)

Tolerance:±0.1(±0.004)



Example for Dielectric Layer



εr,t and W

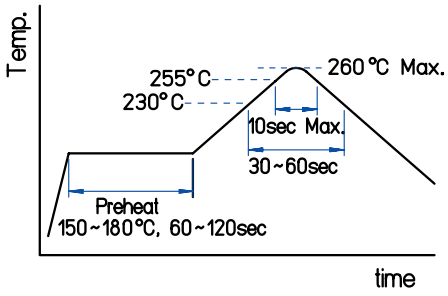
εr \ t	0.3(0.012)	0.4(0.016)	0.5(0.020)
3.5	W=0.44(0.017)	W=0.50(0.020)	W=0.52(0.020)
4.1	W=0.38(0.015)	W=0.46(0.018)	W=0.50(0.020)

SUGGESTED REFLOW SOLDERING CONDITIONS

J-STD-020C Pb-Free Standard

Storage conditions are as per MSL1. These component families are not moisture-sensitive. Baking prior to reflow is not required.

Maximum Cycles: 2x



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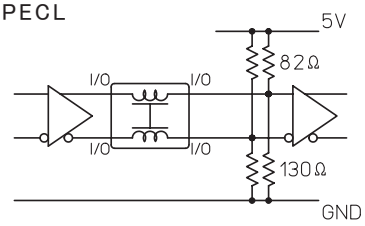
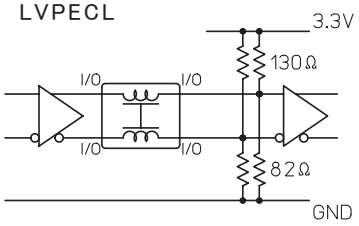
TYPICAL APPLICATIONS AND TERMINATION METHODS

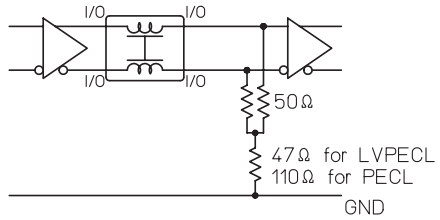
PECL



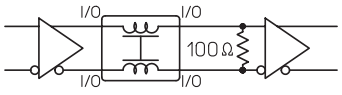
LVPECL



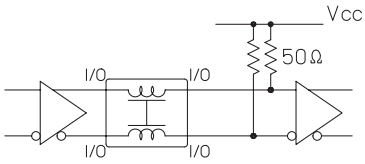
Twisted Pair Termination



LVDS



CML

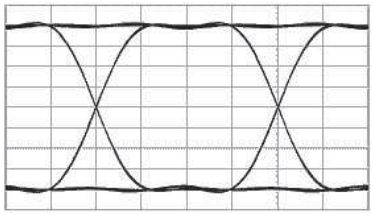


CDLF 0805 Size Differential Chip Delay Line

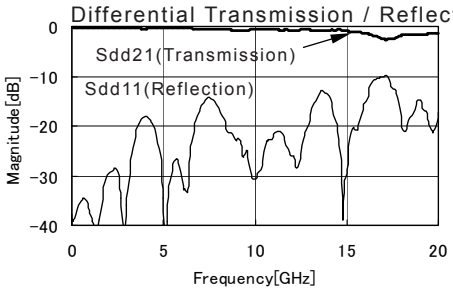
OUTPUT WAVEFORMS (1)

(1) CDLF05C (Actual measurement)

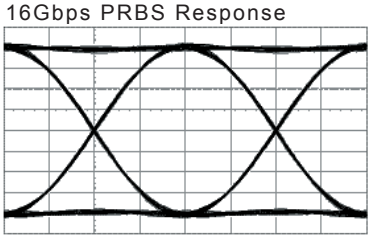
10Gbps PRBS Response



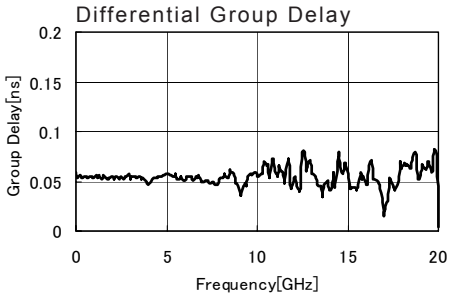
[X-axis: 25ps/Div, Y-axis: 50mV/Div]



16Gbps PRBS Response

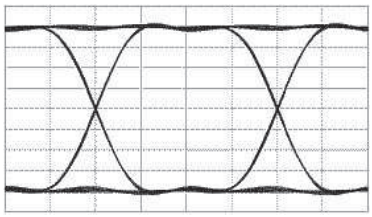


[X-axis: 15.625ps/Div, Y-axis: 50mV/Div]

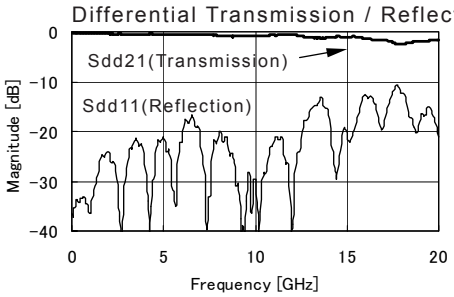


(2) CDLF10C (Actual measurement)

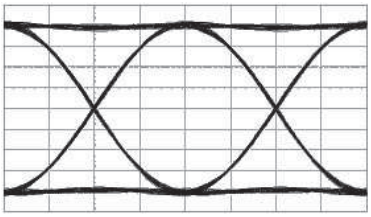
10Gbps PRBS Response



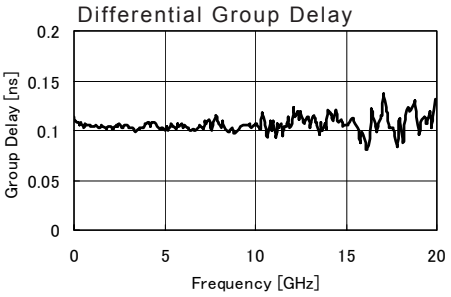
[X-axis: 25ps/Div, Y-axis: 50mV/Div]



16Gbps PRBS Response



[X-axis: 15.625ps/Div, Y-axis: 50mV/Div]



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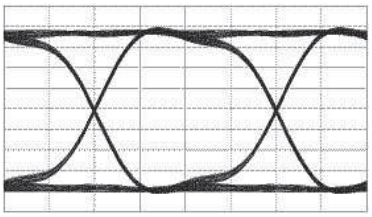
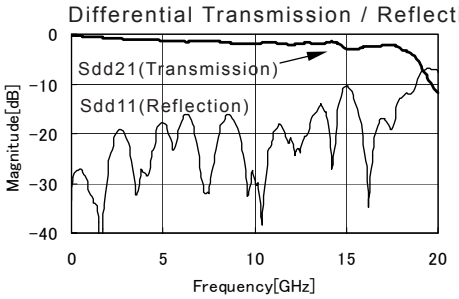
OUTPUT WAVEFORMS (2)

(3) CDLF20C (Actual measurement)

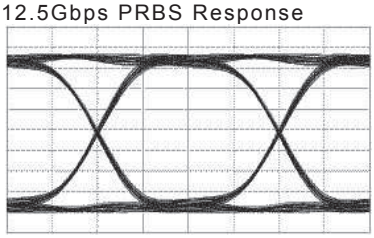
10Gbps PRBS Response



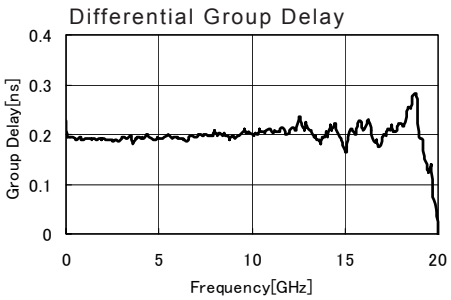
[X-axis: 25ps/Div, Y-axis: 50mV/Div]



12.5Gbps PRBS Response

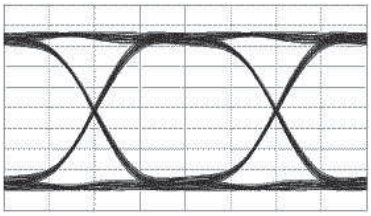


[X-axis: 20ps/Div, Y-axis: 50mV/Div]

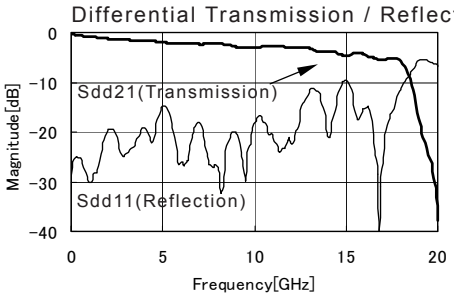


(4) CDLF30C (Actual measurement)

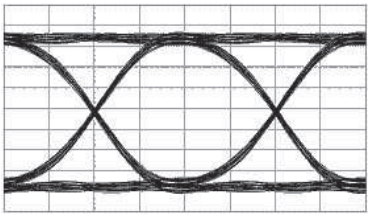
10Gbps PRBS Response



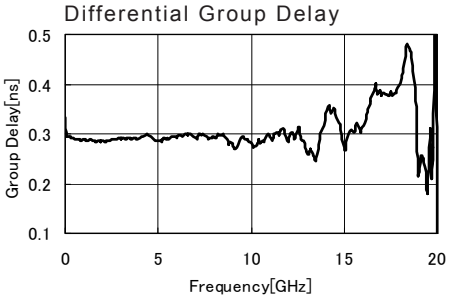
[X-axis: 25ps/Div, Y-axis: 50mV/Div]



12.5Gbps PRBS Response



[X-axis: 20ps/Div, Y-axis: 50mV/Div]



CDLF 0805 Size Differential Chip Delay Line

Technical Note

Within tens of picoseconds of delay time adjustment, a substrate trace can be used for the return circuit. For a 100ps adjustment, either a substrate trace of a coupled differential pair, as shown in Fig.1, or a substrate trace of an uncoupled differential pair, as shown in Fig.2 can be assumed. However, the trace area in either case will become very large. Moreover, as shown in Fig. 1, a time lag arises between the differential pairs due to the imbalance at the corner. Common mode noise will occur at the mid-point, as will the fear of noise radiation. It is very likely that high-quality 10GHz+ band width characteristics cannot be obtained for the circuit shown in Fig.2.

Fig.1 and Fig.2 are verified with an electromagnetic simulator and the characteristics are compared to the results utilizing the CDLF10C. The published Recommended Land Pattern is assumed for the substrate: W=0.38mm, t=0.3mm, and εr=4.1. The underside of the substrate is GND plane.

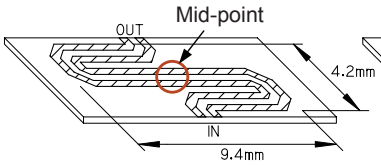


Fig.1 Trace example of a coupled differential pair (Trace area: 40mm²)

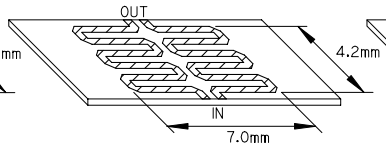


Fig.2 Trace example of an uncoupled differential pair (Trace area: 30mm²)

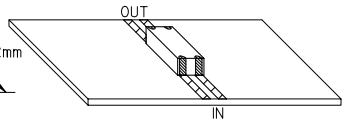
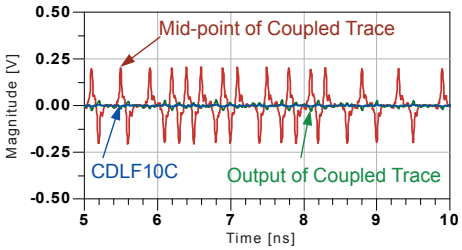


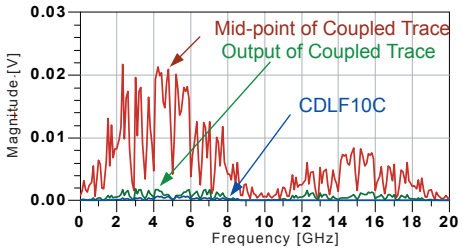
Fig.3 CDLF10C Mounting Image (Footprint: 2.5mm²)

Coupled Trace Comparison (Fig.1) and CDLF10C (Fig.3)

Common-mode Waveform

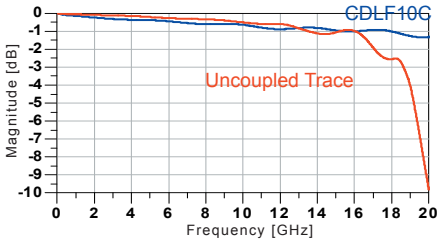


Common-mode Spectrum

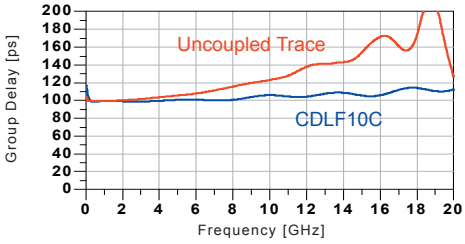


Uncoupled Trace Comparison (Fig.2) and CDLF10C (Fig.3)

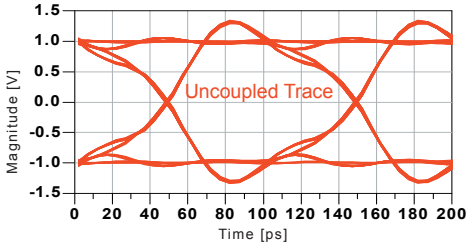
Differential Transmission

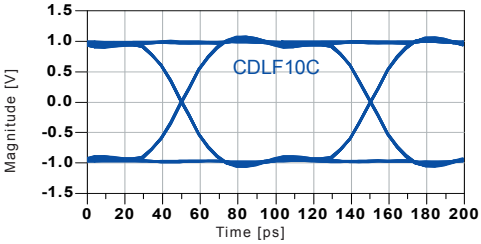


Differential Group Delay



Differential Output Eye-Pattern (10Gbps PRBS, tr/tf=20ps(20%-80%))





ELMEC Technology

Note: Published specifications are subject to change without prior notice.