FDG Low-cost Mid-speed SIP Fixed Delay Lines

Based on ELMEC's expertise in producing High-speed Delay Lines, the FDG-type mid-speed SIP Fixed Delay Line reduces the number of internal elements by 1/3 to 1/2.

FEATURES

- By reducing the number of elements, the Passband will narrow by approx 1/2 compared to the FDC/FDD-types, however, it is also possible to make a comparable reduction in price. If your clock adjustment is within 1/2 of a cycle, the FDG-type should suffice for your needs.
- It is a RoHS-compliant component. The terminals are Nickel with a Tin plating.

COMMON SPECIFICATIONS

Impedance:	FDG1E205: 50Ω±10% Other Parts: 100Ω±10% Components can be designed at 200Ω up to 25ns, and 500Ω up to 10ns. If you are concerned about low power consumption and looking for a higher-impedance Delay Line, please let us know.
Waveform Distortion:	Overshoot/preshoot under ±20%
Temperature Coefficent:	-50 to +200ppm/°C
Insulation Resistance:	DC50V, over 100MΩ
Durable Voltage:	DC50V, 1 minute
Operating Temperature Range:	-40°C to +85°C
Storage Temperature Range:	-40°C to +120°C

SPECIFICATIONS

Part Number	Delay Time	Rise Time (20%-80% Max)	-3 dB Passband (Guarantee)	DC Resistance
FDG1010	1ns±0.2ns	0.6ns	DC～600MHz	1.0Ω Max
FDG2010	2ns±0.2ns	0.6ns	DC～600MHz	
FDG3010	3ns±0.3ns	0.9ns	DC～400MHz	
FDG4010	4ns±0.3ns	1.2ns	DC～300MHz	
FDG5010	5ns±0.4ns	1.4ns	DC～250MHz	1.5Ω Max
FDG6010	6ns±0.5ns	1.8ns	DC～200MHz	
FDG7010	7ns±0.5ns	2.0ns	DC～180MHz	
FDG8010	8ns±0.6ns	2.4ns	DC～150MHz	2.0ΩMax
FDG9010	9ns±0.7ns	2.5ns	DC～140MHz	
FDG10010	10ns±0.7ns	3.0ns	DC～120MHz	
FDG11010	11ns±0.8ns	3.2ns	DC～110MHz	2.5ΩMax
FDG12010	12ns±0.9ns	3.5ns	DC～100MHz	
FDG13010	13ns±1.0ns	3.7ns	DC～95MHz	
FDG15010	15ns±1.1ns	4.2ns	DC～85MHz	
FDG16010	16ns±1.2ns	4.4ns	DC～80MHz	3.0ΩMax
FDG18010	18ns±1.3ns	5.0ns	DC～70MHz	4.0ΩMax
FDG20010	20ns±1.4ns	5.5ns	DC～65MHz	4.5ΩMax
FDG22010	22ns±1.6ns	5.5ns	DC～65MHz	
FDG25010	25ns±1.8ns	7.0ns	DC～50MHz	10.0ΩMax
FDG30010	30ns±2.1ns	9.0ns	DC～40MHz	15.0ΩMax
FDG35010	35ns±2.5ns	10.0ns	DC～35MHz	17.0ΩMax
FDG40010	40ns±2.8ns	12.0ns	DC～30MHz	18.0ΩMax
FDG45010	45ns±3.2ns	14.0ns	DC～25MHz	19.0ΩMax
FDG50010	50ns±3.5ns	18.0ns	DC～20MHz	21.0ΩMax
FDG1E205	100ns±7.0ns	35.0ns	DC～10MHz	

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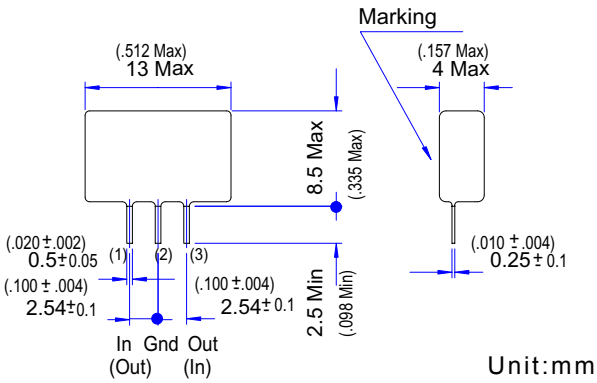
PACKAGE DIMENSIONS & PIN CONFIGURATION



Unit:mm (inch)

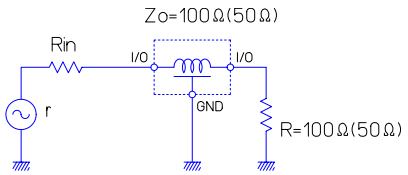
SOLDERING CONDITIONS

Flow Solder 260°C, under 10 seconds

Soldering Iron 350°C, under 5 seconds

TYPICAL APPLICATIONS AND TERMINATION METHODS

(1) Analog circuit



r :Impedance of signal source

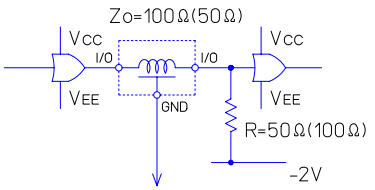
Rin:Input adjustment resistance

Zo :Characteristics impedance of internal Elements (=Output impedance)

Ro :Internal adjustment resistance (=Zo)

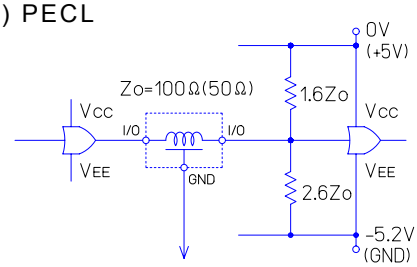
r+Rin=Zo=R

(2) ECL (-2V termination line used)



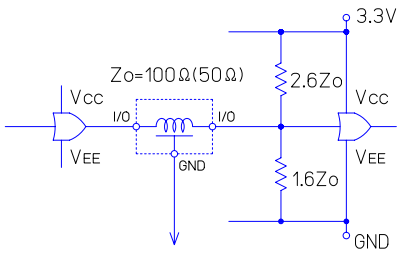
Connect to one of the V_{CC}, V_{EE} or -2V lines

(3) PECL



Connect to either V_{CC} or V_{EE} lines

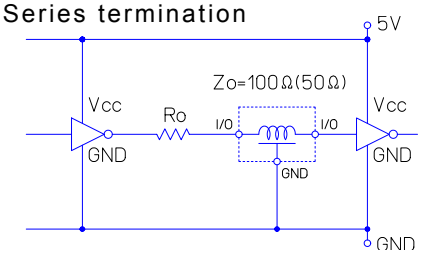
(4) LVPECL



Connect to either 3.3V or GND

(5) TTL(FAST), CMOS(FACT)

Series termination



Ro should be adjusted to a value near Zo.

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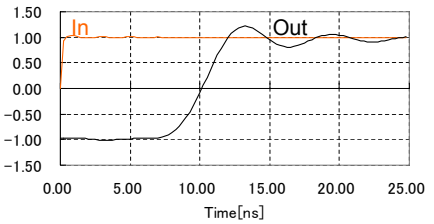
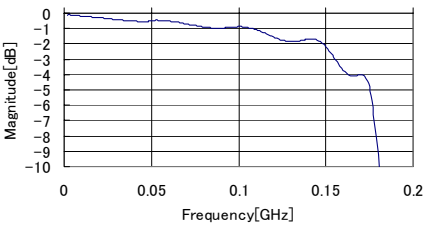
OUTPUT WAVEFORMS (1)

(1) FDG10010

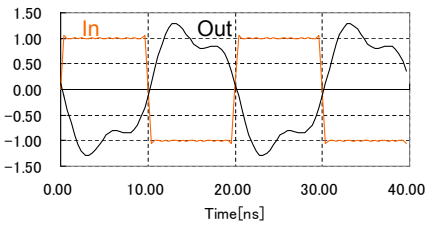
Output waveform (Step function)



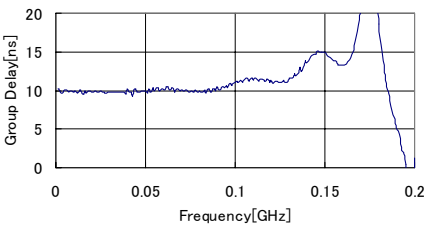
Sdd21 Amplitude / Frequency



Output waveform (50MHz Clock)

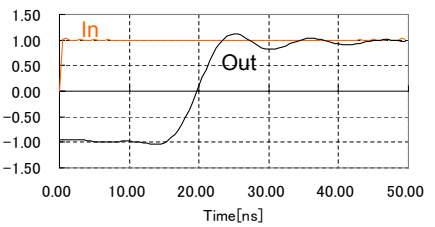


Group Delay

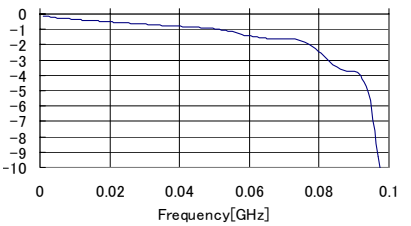


(2) FDG20010

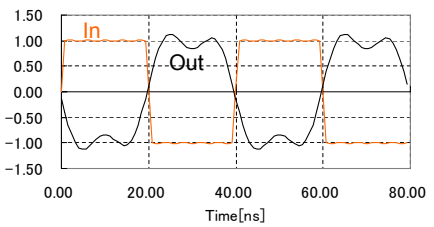
Output waveform (Step function)



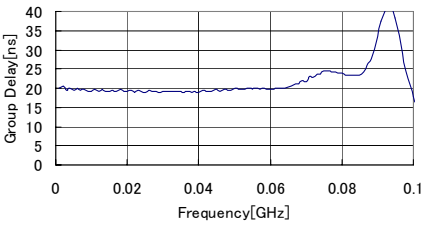
Sdd21 Amplitude / Frequency



Output waveform (25MHz Clock)



Group Delay



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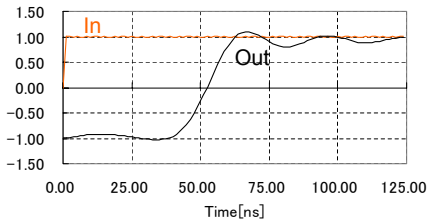
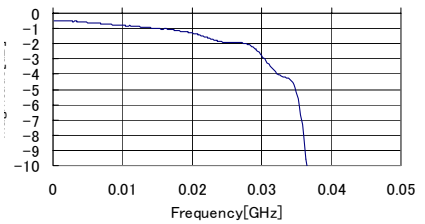
TYPICAL CHARACTERISTICS (2)

(3) FDG50010

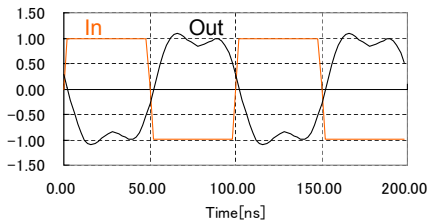
Output waveform (Step function)



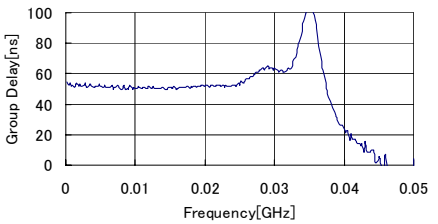
Sdd21 Amplitude / Frequency



Output waveform (15MHz Clock)



Group Delay



RoHS Compliance Status

1. Compliance Status

Completed.

2. Terminal Plating

Base: 100% Ni

External: 100% Sn